REMARKS

Claims ~~1, 3, 5-12, 14, 15, 17, 18, 20, and 24-27 are pending.~~

Claims 1 and 24-27 were rejected under 35 U.S.C. 102(b).

Claims 3-15, 17, 18 and 20 were rejected under 35 U.S.C. 103(a).

Claims 2, 4, 13, 16, 19, and 21-23 are cancelled without prejudice.

No new matter is added.

Applicant request reconsideration and allowance of the claims in view of the remarks below.

Interview Summary

Applicant thanks the Examiner for the brief telephone discussion that was conducted between the Examiner and Applicant's representative, Brian Wichner, on May 18, 2006. During that discussion, Applicant's representative pointed to figures of the reference Deering that appear to teach away from some limitations of the claims. Particularly the limitation that the compare circuit writes to the memory cell array. The Examiner agreed that there may be an issue, and will look further upon receiving applicant's response.

Claim Objections

Applicant has cancelled claim 4. Claim 5 has been amended to depend upon claim 3.

Claim Rejections – 35 U.S.C. § 102

Claims 1 and 24-27 were rejected under 35 U.S.C. 102(b) as being anticipated by Deering U.S. Patent 5,544,306 ("Deering").

Applicant respectfully traverses the rejection.

Claim 1 recites a line connecting the compare circuit to the memory cell array, and a data modifying circuit being adapted to write the external depth data, via the connecting line, into the memory cell array.

The Examiner points to Deering (col. 5, line 66-col. 6, line 4; col. 6, lines 53-62), who teaches that a compare result 240 is transferred over the interleaved rendering bus 64 as the PA_PASS_OUT signal, and writing of the write port data 202 into the pixel buffer 56 (col. 17,

lines 1-10). Though teaching writing into the pixel buffer, Deering fails to teach writing the external depth data, via a connecting line connecting the compare circuit to the memory cell array, into the memory cell array.

Deering, FIG. 2, shows pixel ALU 58 (data modifying circuit) with only one output, line 202, which is to the pixel buffer 56. FIG. 8 shows details of ALU 58. In this figure, compare unit 235 has no output or, in other words, no way of writing data, to the pixel buffer 56. The only line from the ALU 58 to the pixel buffer 56, shown in FIG. 2, is line 202, and line 202 is output by ROP blend units 230-233, not the compare unit 235.

Deering explains that a pixel buffer write enable signal 276, output by the compare unit 235, enables writing of the write port data 202 into the pixel buffer 56 (col. 17, lines 8-10). But one skilled in the art would quickly recognize that an enable signal that enables data to be written is different than the data itself that is written. Thus, Deering does not show or teach writing external depth data via a line connecting the compare circuit to the memory cell array, as claim 1 requires.

The Specification, page 6, line 33, for example, describes an improved time by having, among other elements of the embodiments, the compare circuit 33 adapted to write data to the memory cell array 34 via a line, and without the need of a write enable signal and other components to write the data.

Claim Rejections – 35 U.S.C. § 103

Claims 3-15, 17, 18 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Deering in view of Dowdell U.S. Patent No. 5,301,263 ("Dowdell").

Applicant respectfully traverses the rejection.

Claim 12 recites a compare circuit that is connected via a line to the memory cell array comparing received data, writing from the compare circuit, via the connected line, the external depth data over the corresponding internal depth data into the memory cell array.

These limitations of claim 12 are substantially the same as those in claim 1, as explained above. Thus, Deering fails to anticipate claim 12 for at least the same reasons as discussed for claim 1.

Furthermore, Dowdell does not make up for the shortcomings of Deering. Dowdell does not show, among other things, a line connecting the compare circuit with the memory cell array.

Thus, the combination of Deering and Dowdell fails to render obvious claim 12, and the applicants request withdrawal of the rejection.

Claims 3, 5-11, 14, 15, 17, 18, 20, and 24-27 depend from claims 1 and 12, respectively, and inherently include all of the limitations of their base claims. As discussed above, the prior art does not teach the limitations of their base claim much less the further limitations of the dependent claims. Therefore, these claims are allowable for their dependency and on their own merits. Allowance of these claims is requested.

Conclusion

For the foregoing reasons, reconsideration and allowance of the claims of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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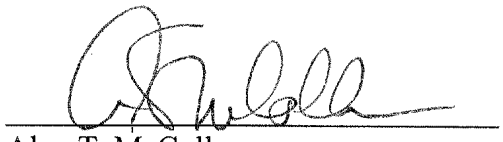

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